**WHAT IS CLAIMED IS**:

1. A method of designing a communication architecture comprising:

a) receiving a partitioned system, communication architecture topology, input traces and performance matrices;

b) analyzing and creating communication analysis graph (CAG);

c) partitioning communication instances to create partition clusters;

d) evaluating cluster statistics related to the partition clusters and assigning parameter values to the partition clusters to form a new system with new communication architecture;

e) reanalyzing the new system and recomputing performance metrics;

f) if performance is improved then synthesizing CATs to realize optimized protocols; and

g) if performance is not improved then returning to step c;

2. The method of claim 1 wherein step c further comprises:

(c) (i) analyzing the CAG to measure impact of individual communication instance delays on system performance;

(c)(ii) measuring performance impact of an instance using sensitivity; and

(c)(iii) grouping instances having a similar impact on system performance into a same partition.

3. The method of claim 2 wherein said sensitivity of the system performance to a communication instance is measured as follows:

perturbing an existing delay of the communication instance by a value;

traversing a transition fanout of the communication instance in the CAG;

recomputing a start and finish time of affected vertices; and

calculating changes in the system performance using recomputed finish times.

4. The method of claim 1 wherein step d is accomplished by deriving a metric that penalizes a partition having a negative impact on delays of communication events in other partitions;

5. The method of claim 4 wherein said metric is calculated as follows:

analyzing the CAG and evaluating for each partition pair $CP_i$ $CP_j$ an amount of time for which communication events that belong to $CP_i$ are delayed due to events from $CP_j$ to form delay statistics ; and

5 combining the delay statistics into a formula that produces an optimum parameter assignment.

6. The method of claim 5 wherein said parameter assignment is done using heuristics.

7. The method of claim 5 wherein said parameter is priority.

8. The method of claim 5 wherein said parameter is DMA block size.

9. The method of claim 5 wherein said parameter assignment takes into account hardware complexity of implementing the parameter.